# APPLICATIONS OF MILLIWATT MICROLOGIC ELEMENTS

By H. T. Chua

## INTRODUCTION

This application note describes the functions and applications of the Fairchild Milliwatt Micrologic Family.* The Milliwatt Micrologic elements possess several distinct features which are of importance to commercial and military applications:

1. Low power
2. High speed
3. Availability of a full gated storage element
4. Reliability of Micrologic

The Milliwatt Micrologic elements are manufactured using the same process as that of the popular Micrologic elements, thus assuring the same high reliability proven in over 32 million hours of operating life test. The basic RTL inverter in the Milliwatt Micrologic elements typically dissipates 2 mW and has a propagation delay of 40 nsec. The d-c ground noise threshold of the circuit is typically 250 mV at 25°C with a fan-out of 4. The worst case noise immunity (see Appendix) is specified at 30 mV when operating between -55°C and 125°C with $V_{CC}$ = 3 V and the circuits fully loaded. Higher specified noise immunity is obtainable by increasing $V_{CC}$ or reducing fan-out, which will be discussed later. A Type-D Flip-Flop (part #913 element) is available which can be used as a shift register or counter.

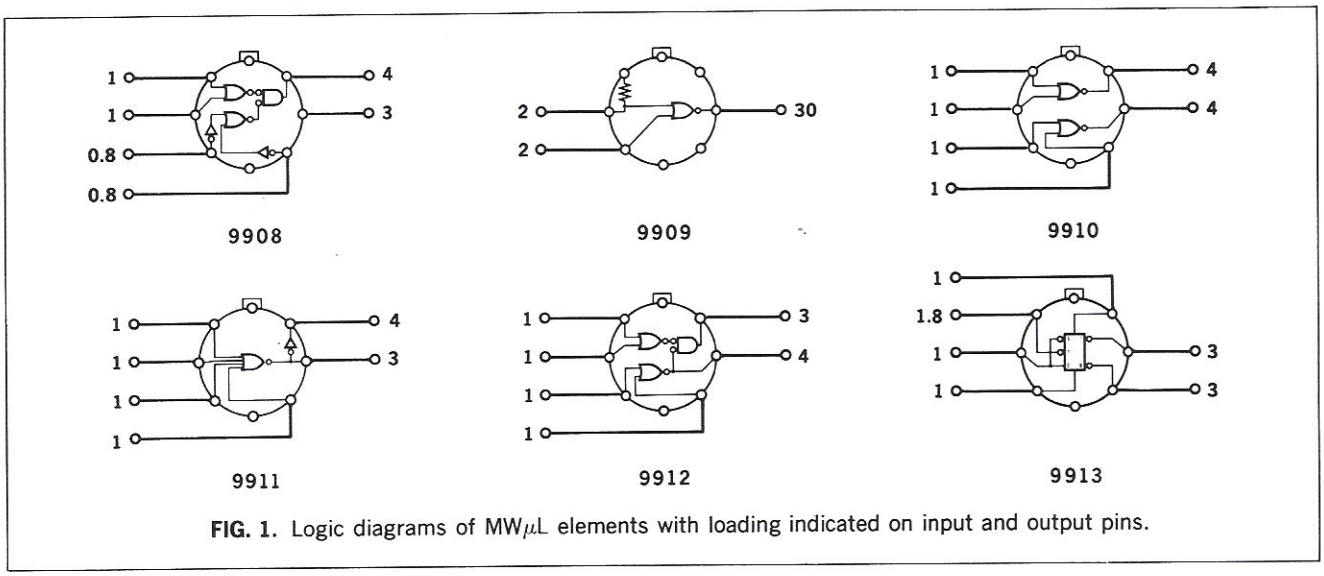



**FIG. 1.** Logic diagrams of MWμL elements with loading indicated on input and output pins.

* As of 1966, "the Milliwatt Micrologic Family" is designated as the "Low Power RTμL" family, and all elements have a four-digit numbering system.

COPYRIGHT, FAIRCHILD SEMICONDUCTOR, 1966 • PRINTED IN U.S.A. 2320-020-126 5M

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

The operating principles of the basic RTL circuit have been described in the Fairchild Technical Papers TP-11, TP-18, and TP-22. *

## The Milliwatt Micrologic Family

The Milliwatt Micrologic Family consists of the following compatible elements:

1. Adder (908 element)
2. Buffer (909 element)
3. Dual gate (910 element)
4. Gate (911 element)
5. Half Adder (912 element)
6. Type-D Flip-Flop (913 element)
7. Expander (921 element)

Typical characteristic curves and loading chart are shown in Figs. 1 and 2. More detailed characteristics of the MW$\mu$L circuits are shown in the Fairchild MW$\mu$L data sheet.

## Adder (908)

The adder performs Mod 2 addition or exclusive OR function; it can also be used to select one of two data streams under the control of a single gate signal.

A full adder may be made from a gate (911) or a dual gate (910), and 2 adder elements, as shown in Fig. 3a. Several full adders may be combined to add 2 multi-bit numbers (Fig. 3b).

An adder connected as a data stream select gate is shown in Fig. 3c. In this circuit, the output D equals A when C is low; and D equals B when C is high

A comparator may be made from an adder element and a dual gate (910), as shown in Fig. 3d. C becomes high when A is not equal to B, and D is the complement of C.

*See also APP-85 and the Micrologic Handbook on related subjects.

## Buffer (909)

The Milliwatt Micrologic Buffer is a low-output-impedance, 2-input inverting driver. The element can supply substantially more output current than the basic RTL circuit to provide higher fan-out or drive capacitive loads. A Milliwatt Micrologic Buffer can drive the clock pulse inputs (pin 1) of 16 Type-D Flip-Flops. It can also drive the input of 3 Micrologic Buffers (900 element) each of whose outputs will drive the clock input of 55 Type-D Flip-Flops.

A resistor is internally connected to one of the inputs of the buffer, which may be connected to the supply voltage if capacitive coupling is desired.

Figure 4a shows 4 buffers (909 element) and 2 capacitors connected as a multivibrator with complementary outputs each capable of driving 30 loads. The typical frequency of oscillation is shown in Fig. 4c. Variation in frequency of $\pm 25\%$ from the typical value should be expected. Pin 3 of any one of the buffers can be used to inhibit the outputs of the multivibrator.

A high-duty-cycle one-shot multivibrator can be made from 2 buffer elements, as shown in Fig. 4d. The first buffer provides large current to charge $C_x$ so that the recovery time of the one-shot is very short. Direct feedback latches up the circuit to make the output pulse width independent of the input pulse width. The output pulse width T is approximately equal to

$$T \approx 0.4\,(R + R_x)\,C_x$$

where

T is in seconds
R is in ohms (3.6 K $\pm 25\%$)
$R_x$ is in ohms
$C_x$ is in farads

and the value of $R_x$ should not exceed 4 K.

If the duty cycle of the one-shot is less than 20%, the first buffer may be replaced by one half of a dual gate (910). If the output load of the one-shot is less than 3, it is more economical to construct the one-shot with a full dual gate, as shown in Fig. 5c.

Gate, Dual Gate and Expander

The gate (911) is a general-purpose 4 input gate with an inverter. It may be used to perform NOR and OR function for positive logic, or NAND and AND function for negative logic.

The dual gate (910) is a pair of 2-input gates, which may be used as a pair of NOR or NAND gates, as a flip-flop with set and reset when cross-connected, or as a double inverter.

A dual gate can be made into an astable multivibrator by adding capacitive feedback and base bias resistors as shown in Fig. 5a. Pin 1 and pin 3 may be used to inhibit the oscillation or grounded if unused.

A dual gate (910) connected as a low-duty-cycle one-shot is shown in Fig. 5c.

A binary-to-decimal decoding matrix can be constructed using eight gates (911) and one dual gate (910), as shown in Figs. 5e and 5f or using eight dual gates and one gate, as shown in Figs. 5d and 5f.

The expander (921) is a dual 2-input gate (910 element) without the collector resistors. Its output terminals may be connected in parallel with those of a dual gate (910) or a gate (911) to increase the fan-in capability of the circuit.

When a dual gate (910) or a gate (911) is used with the expander, the following rules should be observed:

1. Pin 8 of the expander must be connected to $V_{CC}$. This is because in an integrated circuit the resistor is made by diffusing the p-type material into an n-type region. A p-n junction is thus formed, and to prevent current from flowing from the p resistor into the n region, the n region (pin 8) must be connected to a higher potential ($V_{CC}$).

2. The inputs of the expanded gate are increased to 1.33 load due to possible increased current robbing effect when more collectors are connected in parallel.

3. The output current from the expanded gate must be reduced by one half load for every node added because every expander node draws some collector leakage ($I_{CEX}$) current.

Examples of how to use the expander (921) are shown in Fig. 5g.

Half Adder

The half adder (912) is a multipurpose combination of RTL circuits. The configuration is well suited as a half adder, an exclusive OR gate, or any other similar logic construction.

Figure 6 shows the connection of half adder element as a flip-flop with a two-input gate on the set input. Both SET A and SET B must be low in order to set the flip-flop.

Type-D Flip-Flop

The Type-D Flip-Flop (913) is a gated flip-flop used in shift registers and counters. When the clock pulse input (pin 1) changes from "high" to "low," the bit at the data input (pin 2) is gated into the flip-flop. The entry takes place at the time the clock pulse switches. If the data input subsequently changes state, the new bit is not gated in until the next "high"-to-"low" transition of the clock pulse. When the clock pulse is in its "high" state, the flip-flop may be set or cleared by applying a signal to the asynchronous inputs (pin 3 and pin 7).

The Type-D Flip-Flop is a direct-coupled flip-flop. There is no restriction on the rise or fall time of the clock pulse. The data entering two $t_{pd}$'s before and remaining one $t_{pd}$ after the clock pulse switches will be reliably gated into the flip-flop. It takes a maximum of two $t_{pd}$'s to set or clear the flip-flop. A clock pulse of two $t_{pd}$'s wide provides reliable switching. The Type-D Flip-Flop can operate on a 5 Mc clock with a fan-out of 3. Figure 7a shows the input and the output waveforms of a Type-D Flip-Flop operating as a binary counter at a clock rate of approximately 8 Mc.

There is only one synchronous input to the Type-D Flip-Flop. Therefore, although complementary output is provided, only one signal is required to be gated to the next stage. When its complementary output is fed back to the data input, the Type-D Flip-Flop becomes the binary counter as described above.

Figures 7b and 7c show the connections of the Type-D Flip-Flop in two most common usages—shift register and counter. Parallel entry of data into a shift register can be made by gating the data into the set and reset inputs of the Type-D Flip-Flop as shown in Fig. 7d. Data can be entered without first clearing the flip-flop. Control timing should be such that the ENTER pulse occurs when CP input is high.

Special Operating Conditions

The present data sheet provides 100% testing of all elements to guarantee the circuit operation under the following conditions:

1. Circuits operate from -55°C to +125°C.
2. Supply voltage $V_{CC}$ = 3 V
3. Guaranteed minimum noise immunity = 30 mV
4. Each RTL inverter or gate can drive a fan-out of at least 4.

It is possible to operate the elements under different conditions to achieve special operating characteristics. For instance, a fan-out of 5 is obtained at all temperatures when the worst case specified noise margin requirement can be reduced to 5 mV*; a fan-out of higher than 6 is possible when the circuits are operating at 25°C with the same specified noise margin as shown in Fig. 2f.

Figure 2g shows that noise immunity can be increased by increasing $V_{CC}$. A minimum noise immunity of 55 mV is guaranteed at -55°C by operating the circuit at 4.3 V. The same noise immunity is obtainable at +125°C with a $V_{CC}$ of 3.6 V. The 55 mV noise immunity from -55°C to +125°C is guaranteed if the circuits are operated by a sliding power supply having 3.6 V at +125°C and increasing linearly to 4.3 V at -55°C.

The average operating speed is also increased by increasing power supply voltage, as shown in Fig. 2e, and a sliding power supply will tend to equalize the speed at all temperatures.

*Note that noise immunity or noise threshold to ground noise will always be much higher than specified margins, due to the statistical improbabilities of tying together 5 pins, all of which have limit properties.

## APPENDIX

### Specified Noise Immunity and Typical Noise Threshold

The specified noise immunity is the difference between $V_{IN}$ and $V_{ON}$ in the logically high condition and the difference between $V_{OFF}$ and $V_{OUT}$ in the logically low condition.

$V_{IN}$ is the minimum high logic level encountered in the Milliwatt Micrologic system while $V_{ON}$ is the maximum input voltage required to turn on a transistor and bring the collector down to $V_{OUT}$.

$V_{OUT}$ is the maximum output voltage when $V_{ON}$ is applied to the input. $V_{OFF}$ is the maximum voltage applied to the input without turning on the transistor. The worst case condition occurs when a noise voltage $V_N$ appears at the grounding point of gate B, as shown in Fig. 8.

It is seen that the input voltage applied to gate B is $V = V_{IN} - V_N$. If $V_N$ is greater than the specified noise immunity, V will be less than $V_{ON}$ and gate B may or may not turn on. The same noise voltage $V_N$ is also applied to the input of Gate C. Gate C may or may not stay off if

$$V_N + V_{OUT}(\text{gate B}) > V_{OFF}(\text{gate C})$$

Therefore, in order to specify system operation under the worst case condition, the noise $V_N$ should be kept below the specified noise margin.

In order for a system to fail to operate properly due to $V_N$, the following worst case conditions must simultaneously occur:

1. Gate A must be an element which passes $I_{available}$ test marginally.

2. Gates D, E, and F must all be units which pass $I_{IN}$ test marginally and their other inputs must all be high so that they are all drawing maximum current when $V_N$ occurs.

3. Gate B must be an element which passes $V_{ON}$ test marginally.

4. Gate C must be an element which passes $I_{available}$ test marginally.

5. $V_N$ must have the polarity as shown in Fig. 8 and its value is greater than the specified noise immunity.

It is apparent that the probability of having such a worst case arrangement with randomly chosen elements is very low.

A more realistic way of determining noise immunity of a circuit is to measure the typical noise threshold voltage or distribution of the worst parameters thereof. A typical noise threshold voltage measuring circuit is shown in Fig. 9. The elements used are randomly chosen. Gates C, D, and E are all under current hogging condition. A d-c voltage is momentarily applied to "Reset" to turn off gate A. $V_N$ is then slowly increased from zero. When $V_N$ is high enough, gate B can no longer stay on and thus the flip-flop changes state. The noise threshold is the value of $V_N$ shortly before the flip-flop changes state. Figure 2a shows the typical noise threshold voltage measured under various operating conditions. Note that this circuit measures the d-c noise threshold voltage which is the worst type of noise. Pulsed noise threshold is higher than the d-c noise threshold as shown in detail in the MW$\mu$L data sheet.

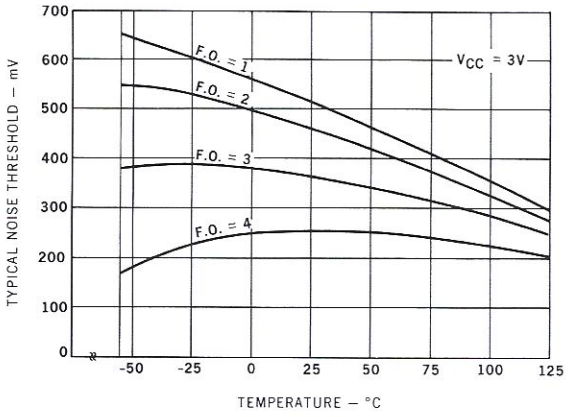



**FIG. 2a.** Typical noise threshold versus temperature.

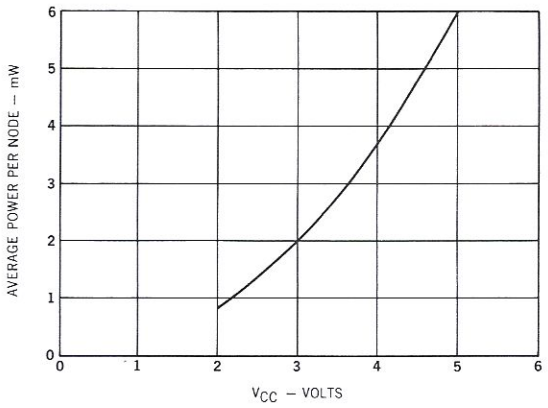



**FIG. 2d.** Average power dissipation per node.

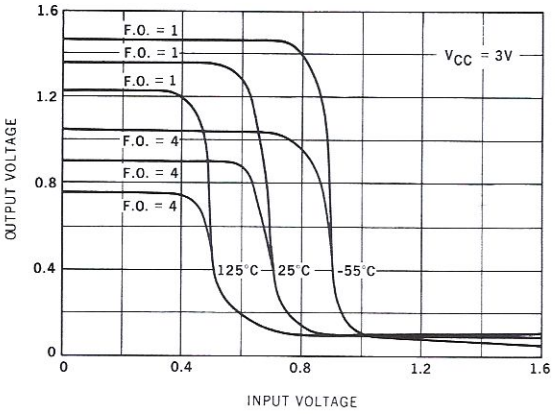



**FIG. 2b.** Input voltage versus output voltage at 3 temperatures.

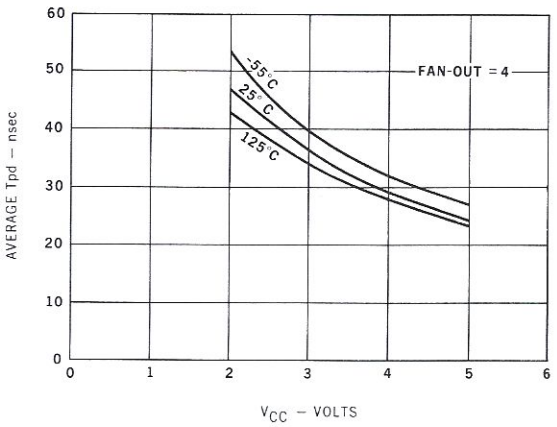



**FIG. 2e.** Average propagation delay time per node versus supply voltage.

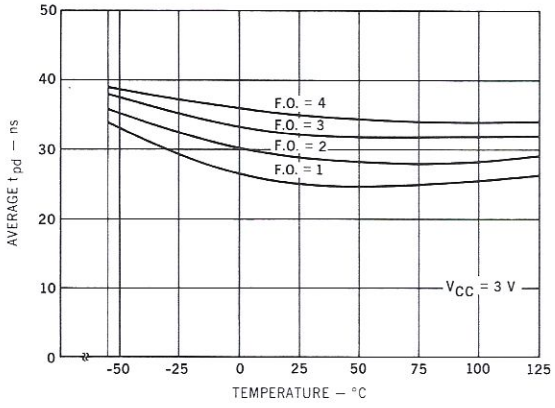



**FIG. 2c.** Average propagation delay time per node versus temperature.

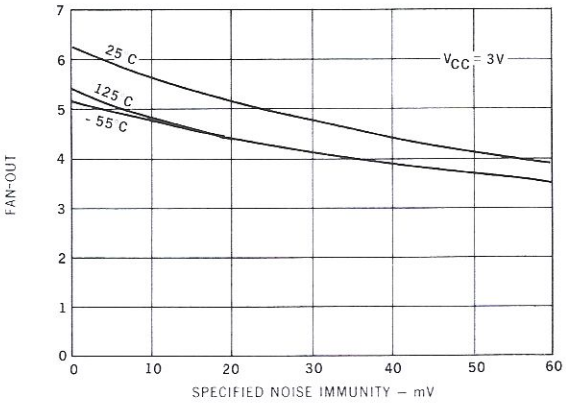



**FIG. 2f.** Specified noise immunity versus fan-out at 3 temperatures.

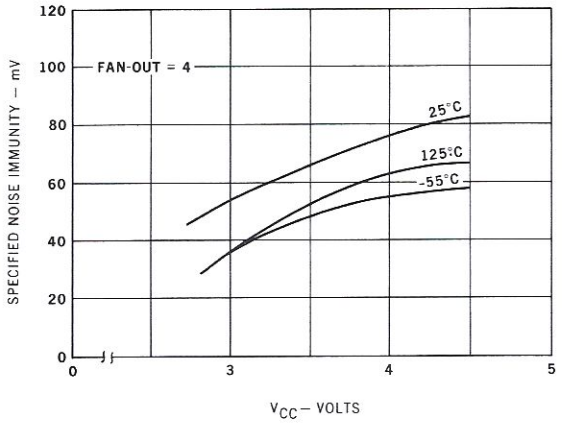



**FIG. 2g.** Specified noise immunity versus supply voltage at 3 temperatures.

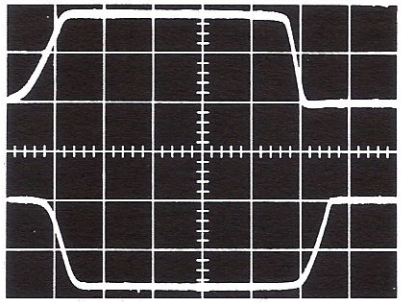


**FIG. 2i.** Waveform of input (top) and output (bottom) of MW$\mu$L gate. Vertical scale: 0.5 V/div. Horizontal scale: 100 ns/div.

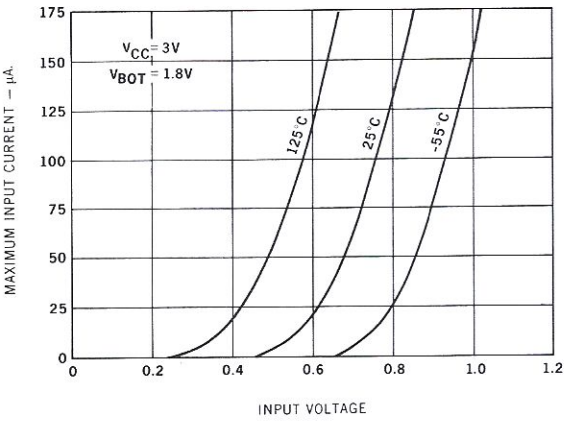



**FIG. 2h.** Maximum input current versus input voltage at 3 temperatures.

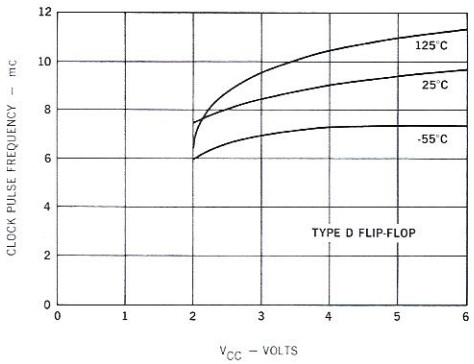
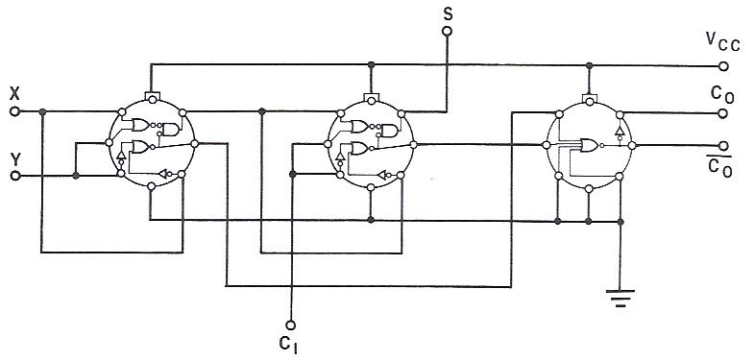



**FIG. 2j.** Clock pulse frequency versus supply voltage at 3 temperatures for Type-D Flip-Flop.




TRUTH TABLE

| X | Y | $C_I$ | $C_O$ | $\overline{C_O}$ | S |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 |

X,Y = DATA INPUTS
$C_I$ = CARRY IN
$C_O$ = CARRY OUT
S = SUM OUT

**FIG. 3a.** Binary full adder with truth table.

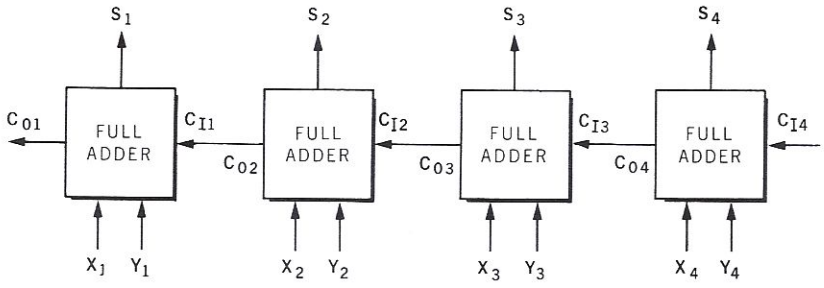
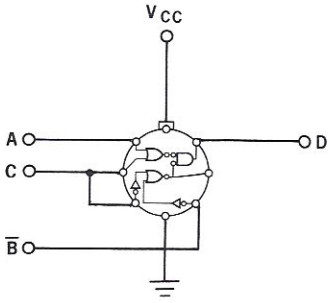
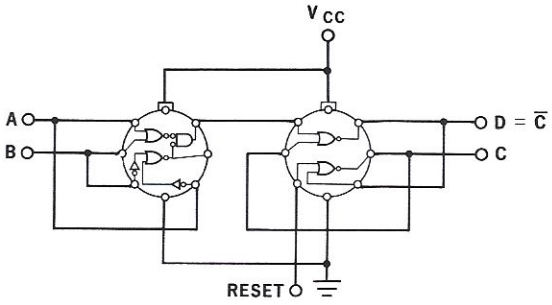



**FIG. 3b.** Full adders adding two multiple-bit numbers.




D = (A + C)(B + $\overline{C}$)
D = A WHEN C = 0
D = B WHEN C = 1
(POSITIVE LOGIC)

**FIG. 3c.** Adder element connected as data stream select gate.




C = 1 WHEN A ≠ B
C = 0 WHEN A = B
(POSITIVE LOGIC)

**FIG. 3d.** Comparator circuit using dual gate and adder elements.

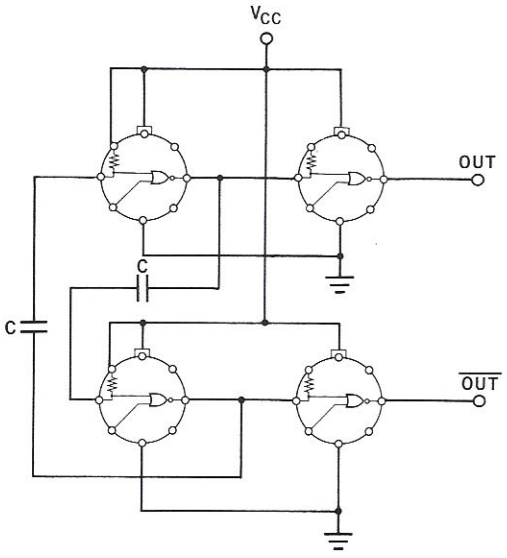



**FIG. 4a.** Four buffer elements connected as free-running multivibrator.

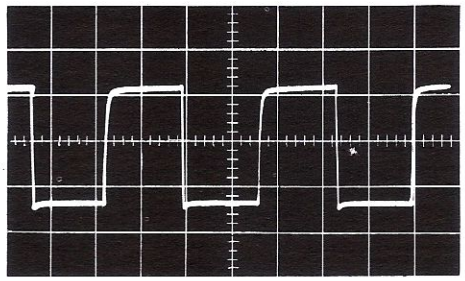


**FIG. 4b.** Output waveform of free-running multivibrator with C = 1000 pf. Vertical scale: 1 V/div. Horizontal scale: 1 $\mu$sec/div.

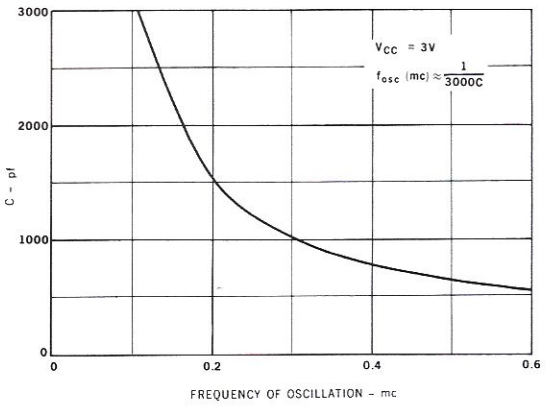



**FIG. 4c.** Capacitance versus frequency of oscillation for free-running multivibrator.

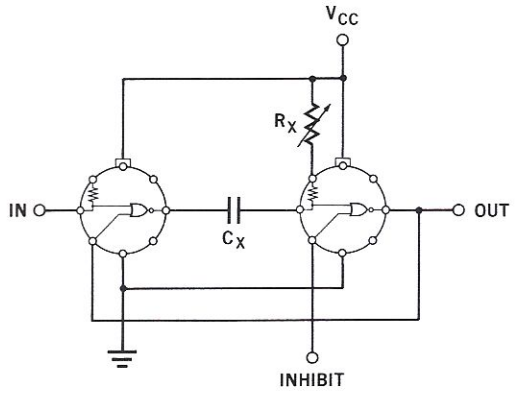



**FIG. 4d.** Buffers used as high-duty-cycle one-shot multivibrator.

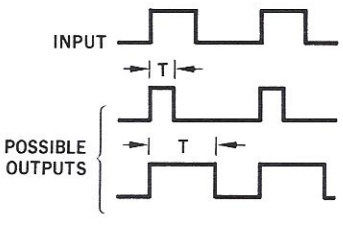



**FIG. 4e.** Input and output waveforms of one-shot multivibrator.

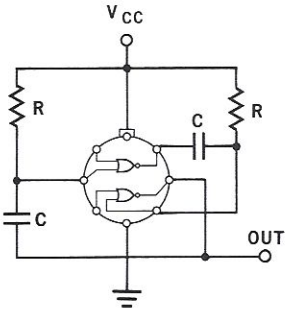



**FIG. 5a.** Single dual gate used as free-running multivibrator.

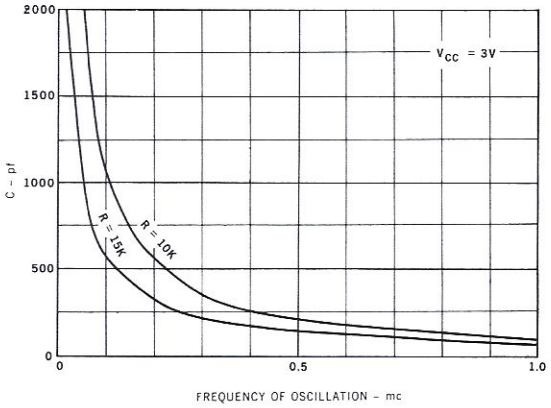
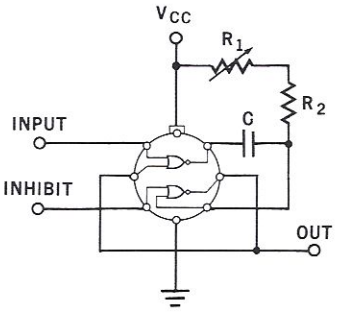
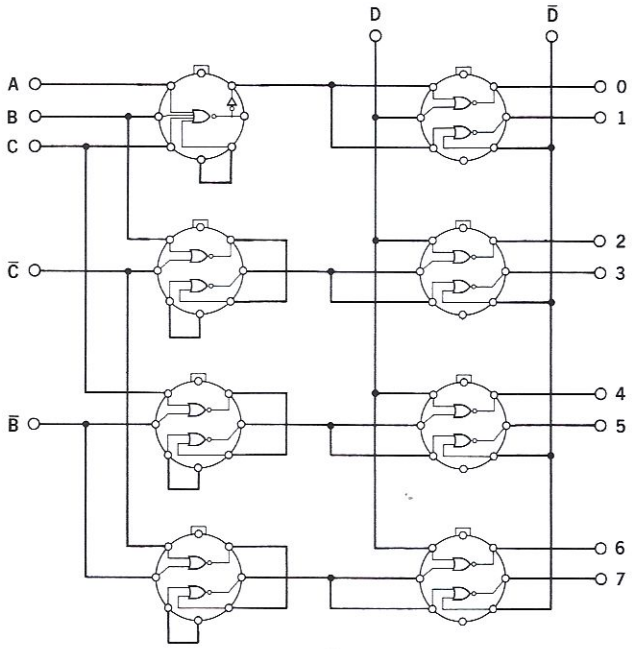



**FIG. 5b.** Capacitance versus frequency of oscillation for free-running multivibrator.

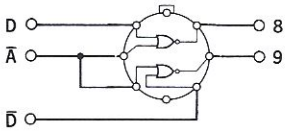



$R_2$ = 3K
$R_1$ ≤12K
C ≥100pf

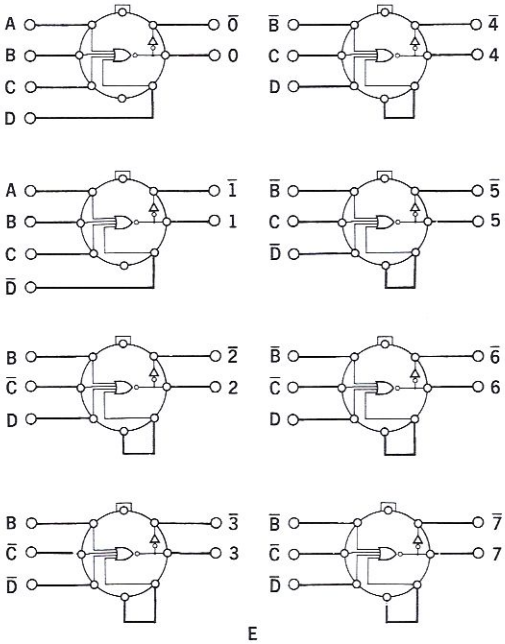
**FIG. 5c.** Single dual gate used as one-shot multivibrator.




D




F




E

| | A | B | C | D |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| * | 1 | 0 | 1 | 0 |
| * | 1 | 0 | 1 | 1 |
| * | 1 | 1 | 0 | 0 |
| * | 1 | 1 | 0 | 1 |
| * | 1 | 1 | 1 | 0 |
| * | 1 | 1 | 1 | 1 |

* NOT ALLOWED

**FIGS. 5d , 5e , 5f.** Binary-to-decimal decoding matrix using gates and dual gates.

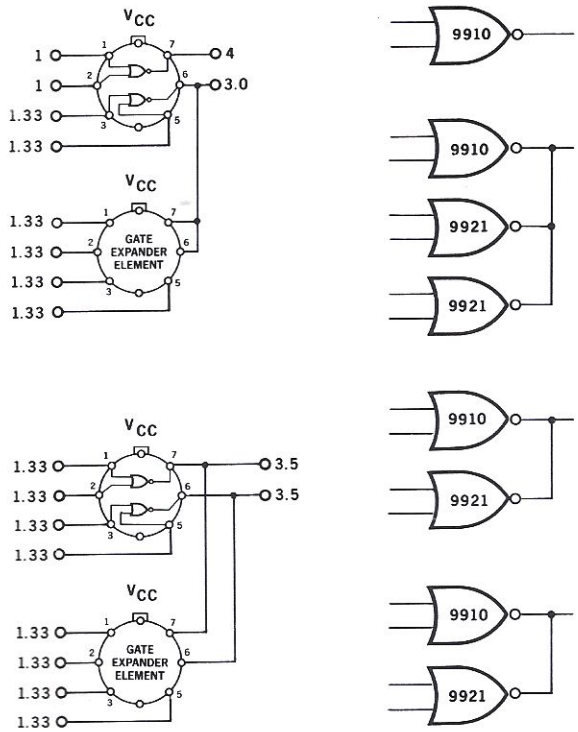



**FIG. 5g.** Expander connected in various ways with dual gate.

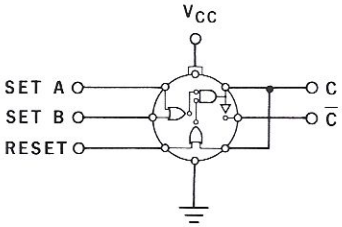



**FIG. 6.** Half adder connected as R-S Flip-Flop.

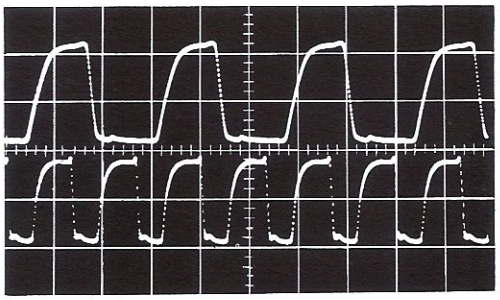


**FIG. 7a.** Waveforms for Type-D Flip-Flop at 25°C and $V_{CC} = 3$ V. Bottom: clock pulse. Top: data output. Vertical scale: 0.5 V/div.; horizontal scale 100 ns/div.

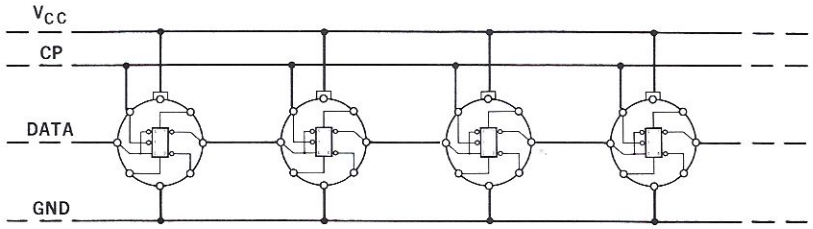



**FIG. 7b.** Shift register stages using Type-D Flip-Flop.

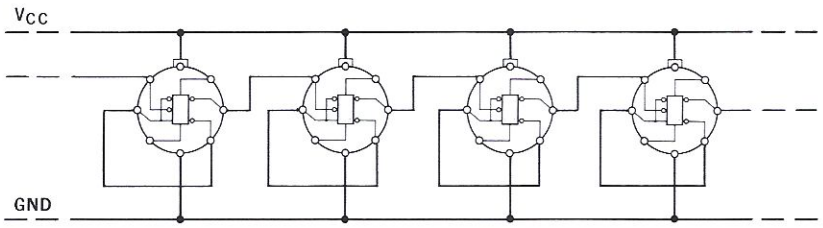



**FIG. 7c.** Binary ripple-carry counter stages using Type-D Flip-Flop.

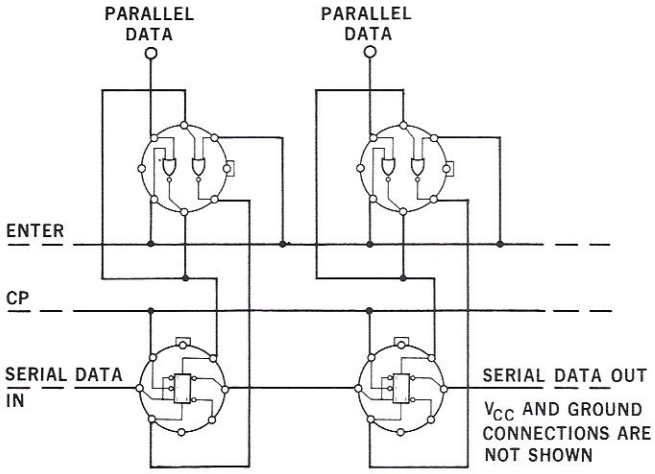



**FIG. 7d.** Method of parallel entry of data into shift register.

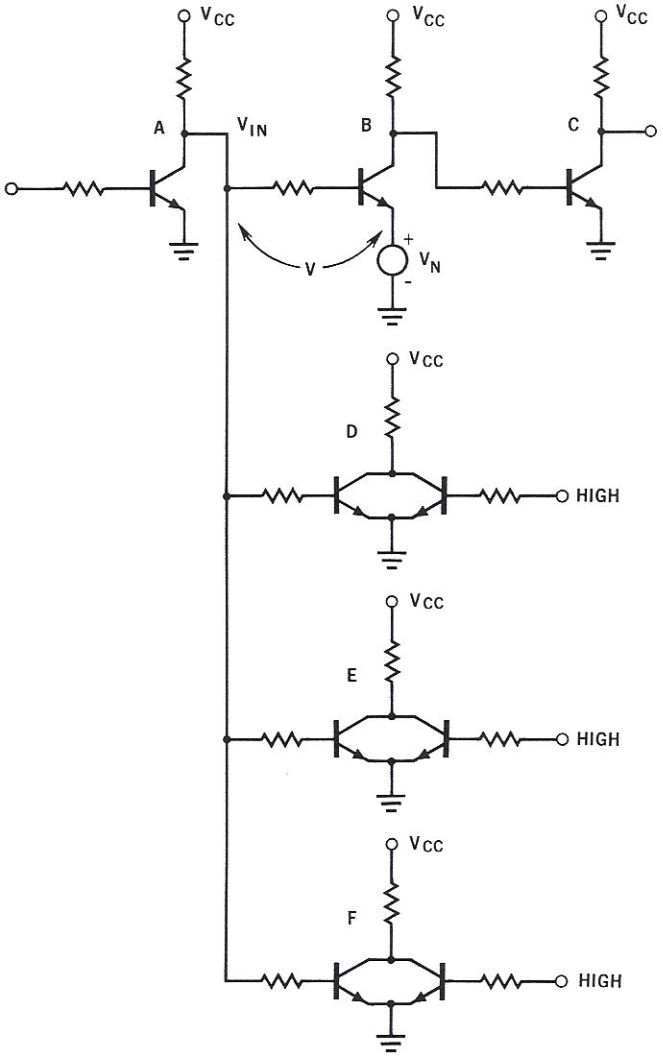



**FIG. 8** Worst-case noise condition.

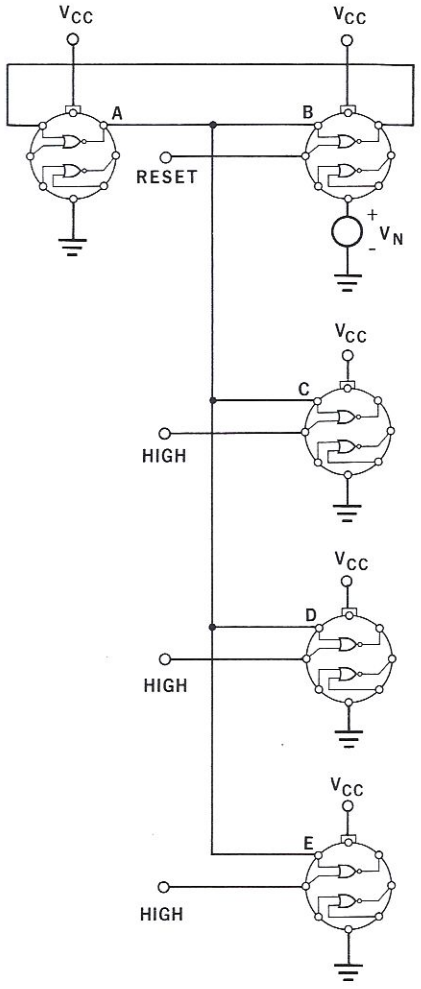



**FIG. 9.** Circuit for measuring noise threshold.